

Microprocessor Supervisory Circuit in 4-Pin SOT143

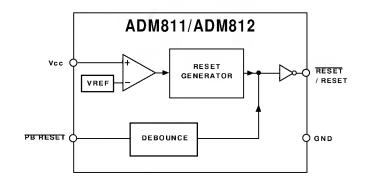
Advance Technical Information

ADM811/ADM812

FEATURES

Superior Upgrade for MAX811/MAX812 Specified Over Temperature Low Power Consumption (6µA typical) Precision Voltage Monitor +3V, +3.3V, +5V Options Reset Assertion Down to 1 V Vcc 140ms min Power-On Reset Logic Low RESET Output (ADM811) Logic High RESET Output (ADM812) Built-in manual reset **APPLICATIONS** Microprocessor Systems Controllers Intelligent Instruments **Automotive Systems** Safety Systems

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

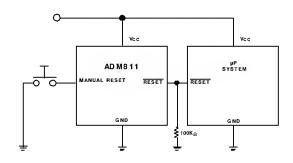
Portable instruments

The ADM811/ADM812 are reliable voltage monitoring devices which are suitable for use in most voltage monitoring applications.

The ADM811/ADM812 is designed to monitor 5 different voltages, each allowing for a 5% or 10% degradation of standard PSU voltages. These voltages have been carefully selected for the effective monitoring of +3V, +3.3V and +5V supply voltage levels.

Included in this circuit is a debounced Manual Reset input. Reset will be activated with an ordinary mechanical switch (or an input from another digital device) or a degredation of the supply voltage. The Manual Reset function is very useful especially if the circuit in which the ADM811/ADM812 is operating in, enters into a state that can only be detected by the user. Allowing the user to manually reset a system can reduce the damage or danger that could be otherwise be caused by an out of control or locked-up system.

TYPICAL OPERATING CIRCUIT



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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A. Tel: 617/329-4700 Fax: 617/326-8703

ADM811/ADM812—SPECIFICATIONS

Parameter	Min	Typ	Max	Units	Test Conditions/Comments
Supply					
Voltage	1.0		5.5	V	$T_A = 0$ °C to +70°C
	1.2			V	$T_A = -40^{\circ}C$ to $+85^{\circ}C$
Current		6	15	μΑ	V_{CC} < 5.5V, ADM81_L/M, I_{out} =0A
		2.7	10	μA	V_{CC} < 3.6V, ADM81_R/S/T, I_{out} =0A
V _{CC} max transient duration		100		μs	T _A =25°C Reset comparator overdrive <2.4V
RESET VOLTAGE THRESHOLD					
ADM81_L	4.54	4.63	4.72	v	$T_A = +25^{\circ}C$
ADM81_L	4.5		4.75	v	$T_A = 0$ °C to +85°C
ADM81_M	4.30	4.38	4.46	v	$T_A = +25^{\circ}C$
ADM81_M	4.25		4.5	v	$T_A = 0$ °C to +85°C
ADM81_T	3.03	3.08	3.14	V	$T_A = +25$ °C
ADM81_T	3.00		3.15	V	$T_A = 0$ °C to +85°C
ADM81_S	2.88	2.93	2.98	V	$T_A = +25$ °C
ADM81_S	2.85		3.00	v	$T_A = 0$ °C to +85°C
ADM81_R	2.58	2.63	2.68	v	$T_A = +25^{\circ}C$
ADM81_R	2.55		2.70	V	$T_A = 0$ °C to +85°C
Reset Threshold Temperature Coef.		30		ppm/°C	
V _{CC} to RESET/RESET Delay		40		μs	$V_{\rm OD} = 125 \text{mV}, \text{ ADM} 81_\text{L/M}$
		20		μs	$V_{OD} = 125 \text{mV}, \text{ADM} 81_R/S/T$
Reset Active Timeout Period	140		560	ms	$V_{CC} = V_{TH(MAX)}$
Manual Reset					
Minimum Pulse Width	10			μs	
Glitch Immunity		100		ns	
RESET/RESET Propagation Delay		0.5		μs	
Pull-up resistance	10	20	30	KW	
The Manual Reset circuit will act on	- 0		•		
An input rising above	2.3			v	$V_{CC} > V_{TH(MAX)}$, ADM81_L/M
An input falling below	2.9		0.8	$\begin{vmatrix} \dot{\mathbf{v}} \end{vmatrix}$	$V_{CC} > V_{TH(MAX)}$, ADM81_L/M
An input rising above	$0.7xV_{\rm CC}$		0.0	v	$V_{CC} > V_{TH(MAX)}$, ADM81_R/S/T
An input falling below	0.714 (66		$0.25 \text{xV}_{\text{CC}}$	$\begin{bmatrix} \dot{\mathbf{v}} \end{bmatrix}$	$V_{CC} > V_{TH(MAX)}$, ADM81_R/S/T
			0.2311100	,	VCC - VIH(MAX), 11211201_1VG, 1
RESET Output Voltage			0.2	\ _V	V - V I - 12A
Low (ADM812R/S/T)			0.3	V	$V_{CC} = V_{TH(MAX)}$, $I_{SINK} = 1.2\text{mA}$
Low (ADM812L/M)	0.017		0.4	V	$V_{CC} = V_{TH(MAX)}, I_{SINK} = 3.2\text{mA}$
High(ADM812R/S/T/L/M)	$0.8V_{\rm CC}$		0.2	V	$1.8V < V_{CC} < V_{TH(MIN)}, I_{SINK} = 150 \mu A$
Low (ADM811R/S/T)			0.3	V	$V_{CC} = V_{TH(MIN)}, I_{SINK} = 1.2mA$
Low (ADM811L/M)			0.4	V	$V_{CC} = V_{TH(MIN)}$, $I_{SINK} = 3.2mA$
Low (ADM811R/S/T/L/M)	0.011		0.3	V	$V_{CC}>1.0V$, $I_{SINK}=50\mu A$
High (ADM811R/S/T)	$0.8V_{\rm CC}$			V	$V_{CC} > V_{TH(MAX)}$, $I_{SOURCE} = 500\mu A$
High (ADM811L/M)	$V_{\rm CC}$ -1.5			l V l	$V_{CC} > V_{TH(MAX)}$, $I_{SOURCE} = 800 \mu A$

ABSOLUTE MAXIMUM RATINGS*

 $(T_A = +25^{\circ}C \text{ unless otherwise noted})$

Terminal Voltage (with respect to ground)

V _{CC} 0.3 V to +6 V
All other inputs0.3 V to Vcc + 0.3 V
Input Current
V _{CC} 20 mA
<u>MR</u> 20mA
Output Current
RESET, RESET 20 mA

Power Dissipati	on $(1_A$	\ = +	-70°C),	
RT-3 SOT23				
	TTTT 10 00	•	=000	

Derate by 4mW/°C above 70°C

Operating temperature range-40°C to +85°C

Storage temperature range-65°C to +160°C Lead Temperature (Soldering, 10 secs) +300°C Vapor Phase (60 secs)+215°C Infrared (15 secs) +220°C

^{*}Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

Typical Performance Characteristics

Figure 2. Supply Current vs. Temperature (ADM81_R/S/T) (No Load) Figure 3. Supply Current vs. Temperature (ADM81_L/M) (No Load) Figure 4. Power-Down RESET

Delay vs. Temperature

(ADM81_R/S/T)

Figure 5. Power-Down RESET Delay vs. Temperature ADM8_L/M Figure 6. Power-Up Reset Timeout vs. Temperature Figure 7. Reset Threshold Deviation vs. Temperature

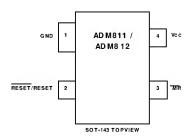
Figure 8. Reset Output Voltage vs. Supply Voltage

Figure 9. Maximum Transient Duration Without causing a Reset Pulse vs. Reset Comparator Overdrive. Figure 10. Power-Up RESET Active Time vs. Temperature

Advance Technical Information

PIN FUNCTION DESCRIPTION

Pin	Mnemonic	Function
1	GND	0 V. Ground reference for all signals.
2	RESET(ADM811)	Active Low Logic Output. RESET remains low while V_{CC} is below the reset threshold or when \underline{MR} is low, RESET then remains low for 240ms (typ) after V_{CC} rises above the reset threshold
2	RESET(ADM812)	Active High Logic Output. RESET remains high while $V_{\rm CC}$ is below the reset threshold or when \underline{MR} is low, RESET then remains high for 240ms (typ) after $V_{\rm CC}$ rises above the reset threshold
3	MR	Manual Reset. This active low debounced input will ignore input pulses of 100ns or less (typical) and is guaranteed to accept input pulses of greater than 10µs. Leave floating when not used.
4	V_{CC}	+3V, +3.3V or +5V monitored supply voltage.



PIN CONFIGURATION

Table I. Reset Threshold Options

Model	RESET Threshold
ADM811LART	4.63 V
ADM811MART	4.38 V
ADM811TART	3.08 V
ADM811SART	2.93 V
ADM811RART	2.63 V
ADM812LART	4.63 V
ADM812MART	4.38 V
ADM812TART	3.08 V
ADM812SART	2.93 V
ADM812RART	2.63 V

CIRCUIT INFORMATION

RESETTHRESHOLDS

The reset output provides a <u>RESET</u> (for the ADM811) or a RESET (for the ADM812) output to the microprocessor whenever the V_{CC} input is below the reset threshold. The actual reset threshold is dependant on whether a L, M, T, S or R suffix is used. Please refer to Table 1.

RESETOUTPUT

On power-up and after V_{CC} rises above the reset threshold, an internal timer holds the reset output active for 240ms . This is intended as a power-on reset signal for the processor. It allows time for both the power supply and the microprocessor to stabilize after power-up. If a power supply brownout or interruption occurs, the reset output is similarly activated and remains active for 240ms after the supply recovers. This allows time for the power supply and microprocessor to stabilize.

The ADM811 provides an active low reset output (RESET) while the ADM812 provides an active high output (RESET)

On the ADM811, during power-down, the <u>RESET</u> output remains valid (low) with V_{CC} as low as 1 V. This ensures

that the microprocessor is held in a stable shutdown condition as the supply falls and also ensures that no spurious activity can occur via the μP as it powers up.

MANUAL RESET

The ADM811 and ADM812 are equiped with a manual reset input. This input is designed to operate in a noisey environment where unwanted glitches could be induced. These glitches could be produced by the bouncing action of a switch contact or where a Manual Reset switch may be located some distance away from the circuit (the cabeling of which may pick up noise)

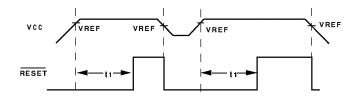
The Manual Reset input is guaranteed to ignore logically valid inputs which are faster than 100ns and accept inputs longer in duration than 10μ s.

GLITCH IMMUNITY

The ADM811/ADM812 contains internal filtering circuitry providing glitch immunity for fast transient glitches on the power supply line. Figure 9 shows the comparator response time for short transients.

Advance Technical Information

ADM811/ADM812



t1 = RESET TIME = 240MS TYP. VREF = RESET VOLTAGE THRESHOLD

Figure 1. Power Fail Reset Timing

INTERFACING TO OTHER DEVICES

OUTPUT

The ADM811 and ADM812 series is designed to integrate with as many devices as possible. One feature of the ADM811 and ADM812 is the reset output which is directily proportional to $V_{\rm cc}$ (this is guaranteed only while $V_{\rm cc}$ is greater than 1V). This enables the part to be used in both 3V and 5V or any Nominal Voltage within the Minimum and Maximum Specifications for $V_{\rm cc}$.

Because of this design approach, the ADM811 and ADM812 is capable of operating correctily in any circuit where the reset output voltages are required to be between ground or $V_{\rm cc.}$

THE BENEFITS OF A VERY ACCURATE RESET THRESHOLD

In other Microprocessor Reset Circuits, tolerances in supply voltages can lead to an overall increase in Reset tolerence levels due to inappropriate power supply levels at the Microprocessor supervisory circuit power supply. Because the ADM811 and ADM812 series can operate effectively even when there are large degradations of the supply voltages, the possibility

of a malfunction during a power failure is greatly reduced. Another advantage of the ADM811 and ADM812 Series is its very accurate internal voltage reference circuit. Combined, these benifits produce an exceptionally reliable Microprocessor Supervisory Circuit.

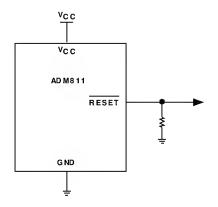


Figure 10. Ensuring a Valid Reset Output Down to V_{cc} =0V

ENSURING A VALID RESET OUTPUT DOWN TO $V_{\rm CC} \text{=-} 0\,\text{V}$

When Vcc falls below 0.8V, ADM811s <u>RESET</u> no longer sinks current. Therefore a high impedance CMOS logic input connected to Reset may drift to undetermined logic levels. To eliminate this problem a 100KW Resistor should be connected from <u>RESET</u> to ground.

ORDERING GUIDE

Model*	Reset Threshold	Temperature Range	Brand Information	Quantity
ADM811LART-REEL	4.63 V	-40°C to +85°C	9LXX	10K
ADM811LART-REEL-7	4.63 V	−40°C to +85°C	9LXX	3K
ADM811MART-REEL	4.38 V	−40°C to +85°C	9MXX	10K
ADM811MART-REEL-7	4.38 V	−40°C to +85°C	9MXX	3K
ADM811TART-REEL	3.08 V	−40°C to +85°C	9TXX	10K
ADM811TART-REEL-7	3.08 V	−40°C to +85°C	9TXX	3K
ADM811SART-REEL	2.93 V	−40°C to +85°C	9SXX	10K
ADM811SART-REEL-7	2.93 V	−40°C to +85°C	9SXX	3K
ADM811RART-REEL	2.63 V	−40°C to +85°C	9RXX	10K
ADM811RART-REEL-7	2.63 V	−40°C to +85°C	9RXX	3K
ADM812LART-REEL	4.63 V	−40°C to +85°C	ALXX	10K
ADM812LART-REEL-7	4.63 V	−40°C to +85°C	ALXX	3K
ADM812MART-REEL	4.38 V	−40°C to +85°C	AMXX	10K
ADM812MART-REEL-7	4.38 V	−40°C to +85°C	AMXX	3K
ADM812TART-REEL	3.08 V	−40°C to +85°C	ATXX	10K
ADM812TART-REEL-7	3.08 V	−40°C to +85°C	ATXX	3K
ADM812SART-REEL	2.93 V	−40°C to +85°C	ASXX	10K
ADM812SART-REEL-7	2.93 V	−40°C to +85°C	ASXX	3K
ADM812RART-REEL	2.63 V	−40°C to +85°C	ARXX	10K
ADM812RART-REEL-7	2.63 V	−40°C to +85°C	ARXX	3K

^{*}Only available in Reels.

ADM811/ADM812

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-6- Rev 1.0 3/97